U.S.S.N. 10,797,945

Claim Amendments

Please amend claims 18, 21, 32, and 38 and 40-42 as follows:

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Listing of Claims

Claims 1-17 (cancelled)

18. (currently amended) A contact interconnect structure comprising:

a semiconductor substrate comprising CMOS devices including active contact regions;

a first contact layer overlying the active contact regions comprising a first plurality of metal filled openings extending through the first contact layer thickness to the active contact regions;

a second contact layer overlying the first contact layer comprising a second plurality of metal filled openings, each of said second plurality of metal filled openings extending through the second contact layer thickness to a respective one or more of the first plurality of metal filled openings;

wherein, ~~each of~~ the first plurality and the second plurality of metal filled openings form a physically continuous contact interconnect structure having an aspect ratio of less than about 4.5 with respect to a respective contact layer.

19. (previously presented) The contact interconnect structure of claim 18, wherein the bottom portion of said contact interconnect

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structure has a maximum width of less than about 70 nanometers and an aspect ratio of less than about 4.5.

20. (previously presented) The contact interconnect structure of claim 18, further comprising an overlying metallization layer in electrical communication with the second plurality of metal filled openings.

21. (currently amended) The contact interconnect structure of claim 18, wherein the first and second contact layers ~~comprise~~ are selected from the group consisting of PETEOS, BPTEOS, BTEOS, PTEOS, TEOS, PEOX, nitrogen doped silicon oxide, fluorine doped silicon oxide, SiC, silicon nitride, and silicon oxynitride~~, or combinations thereof~~.

22. (previously presented) The contact interconnect structure of claim 18, wherein the first and second contact layers comprise lowermost portions selected from the group consisting of silicon carbide, nitrogen doped silicon oxide, silicon nitride, and silicon oxynitride.

23. (canceled)

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24. (original) The contact interconnect structure of claim 18, wherein the first and second first and second plurality of metal filled openings comprise conductive materials selected from the group consisting of Cu, W, Al, AlCu, TiN, TiW, Ti, TaN, and Ta.

25. (original) The contact interconnect structure of claim 18, wherein the active contact regions are selected from the group consisting of source and drain regions and gate electrodes.

26. (previously presented) The contact interconnect structure of claim 25, wherein the gate electrode comprises a gate structure having a gate length of less than about 45 nm.

27. (original) The contact interconnect structure of claim 18, wherein the active contact regions comprise a conductive material selected from the group consisting of Ti, Co, Ni, Pt, W, $TiSi_2$, $CoSi_2$, NiSi, PtSi, WSi_2, TiN, and TaN.

28. (previously presented) The contact interconnect structure of claim 18, wherein the first and second contact layers comprises an uppermost portion selected from the group consisting of a hardmask layer and a BARC layer.

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29. (original) The contact interconnect structure of claim 18, wherein the first and second plurality of metal filled openings comprise a shape selected from the group consisting of circular and rectangular.

30. (previously presented) The contact interconnect structure of claim 18, wherein the first and second plurality of metal filled openings are selected from the group consisting of vias, contact holes, butt contact interconnects, local interconnects, and interconnect lines.

31. cancelled

32. (currently amended) A contact interconnect structure comprising:

at least first and second stacked contact layers comprising a respective first and second plurality of metal filled openings extending through the first and second contact layers to a contact region comprising an active transistor region to form a physically connected stacked contact interconnect structure;

wherein, ~~each of~~ the ~~at least~~ first plurality and the second plurality of metal filled openings comprise a bottom portion

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having a maximum width of less than about 70 nanometers and an aspect ratio of less than about 3.3 with respect to a respective contact layer.

33. (previously presented) The contact interconnect structure of claim 32, wherein the bottom portion has a maximum width of less than about 50 nanometers and an aspect ratio of less than about 4.5.

34. (previously presented) The contact interconnect structure of claim 32, wherein the first and second contact layers comprise an underlying-etch stop layer.

35. (previously presented) The contact interconnect structure of claim 32, wherein the active transistor region is selected from the group consisting of source and drain regions and gate electrodes.

36. (original) The contact interconnect structure of claim 35, wherein the gate electrode comprises a gate structure having a gate length of less than about 45 nm.

37. (original) The contact interconnect structure of claim 32,

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wherein the overlying conductive regions comprise a metallization layer.

38. (currently amended) A stacked contact interconnect structure for achieving a high aspect ratio comprising:

a semiconductor substrate comprising CMOS devices including active contact regions;

a first contact layer overlying the active contact regions comprising a first metal filled opening extending through the first contact layer thickness to the active contact regions;

a second contact layer overlying the first contact layer comprising a second metal filled opening extending through the second contact layer thickness to the first metal filled opening[[s]];

wherein, each of the first and second metal filled openings have about the same width to form a physically connected stacked contact interconnect structure having an aspect ratio of less than about 4.5 with respect to a respective contact layer.

39. (previously presented) The contact interconnect structure of

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claim 36, wherein the bottom portion of said contact interconnect structure has a maximum width of less than about 70 nanometers and an aspect ratio of less than about 4.5.

40. (currently amended) The contact interconnect structure of claim 36, wherein the first and second contact layers ~~comprise~~ are selected from the group consisting of PETEOS, BPTEOS, BTEOS, PTEOS, TEOS, PEOX, nitrogen doped silicon oxide, fluorine doped silicon oxide, SiC, silicon nitride, and silicon oxynitride~~, or combinations thereof~~.

41. (currently amended) The contact interconnect structure of claim 36, wherein the first and second contact layers each comprise a lowermost etch stop layer selected from the group consisting of silicon carbide, nitrogen doped silicon oxide, silicon nitride, and silicon oxynitride.

42. (currently amended) The contact interconnect structure of claim 36, wherein the first plurality and ~~second first and~~ the second plurality of metal filled openings comprise conductive materials selected from the group consisting of Cu, W, Al, AlCu, TiN, TiW, Ti, TaN, and Ta.

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43. (previously presented) The contact interconnect structure of claim 36, wherein the active contact regions are selected from the group consisting of source and drain regions and gate electrodes.

44. (previously presented) The contact interconnect structure of claim 36, wherein the active contact regions comprise a conductive material selected from the group consisting of Ti, Co, Ni, Pt, W, $TiSi_2$, $CoSi_2$, NiSi, PtSi, WSi_2, TiN, and TaN.

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